

## Cross-Reference to Related Applications

This continuation application claims priority from currently pending U.S. Patent Application Serial No. 10/202,556, entitled "Method and Apparatus for Regulating Predriver for Output Buffer," filed July 23, 2002, and hereby incorporated herein by reference.

## In the Specification

Please replace paragraph [0014] as follows:

Figure 2 illustrates [a] an I-V diagram for operation for a pull-down transistor device configured with a prior art predriver circuit;

Please replace paragraph [0015] as follows:

Figure 3 illustrates an exemplary embodiment of an electronic system with a memory system in accordance with the present invention;

Please replace paragraph [0018] as follows:

Figure 10 illustrates an I-V diagram for operation for a pull-down element configured with a regulated predriver for an output buffer in accordance with an exemplary embodiment of the present invention.

Please replace paragraph [0040] as follows:

In addition, with reference to an output buffer 700 illustrated in Figure 7, a limiter circuit 706 can also be configured in [an] a p-channel diode clamp arrangement. Limiter circuit 706 comprises one or more p-channel devices connected in a diode manner, e.g., p-channel transistors M<sub>P1</sub>, M<sub>P2</sub>, and M<sub>P3</sub>. Again, gate voltage V<sub>GATE</sub> is limited by the number of P-channel devices times the threshold voltage V<sub>TP</sub>, e.g., for 3 x V<sub>TP</sub>, with a threshold voltage V<sub>TP</sub> = 0.9 volts, V<sub>GATE</sub> is limited to 2.7 volts. Still further, instead of using diode-connected p-channel or n-channel transistors, with reference to an output buffer 800 illustrated in Figure 8, a limiter circuit 806 can also be

configured with one or more diodes, e.g., diodes D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub> and D<sub>4</sub>. Thus, for four diodes and a threshold voltage V<sub>TH</sub> =0.7 volts, V<sub>GATE</sub> is limited to 2.8 volts.